REMARKS

Applicants respectfully acknowledge the Examiner's consideration of their Amendment of 15 April 2004 in the above-identified application and request reconsideration of the subject application based on the following Remarks detailing the Examiner's erroneous attribution of certain inherent disclosure to the cited Ino reference and the Examiner's misunderstanding of certain of the arguments previously submitted.

Claims 1-8 and 10-21 are pending in the subject application.

Claims 1-8 and 10-21 stand rejected under 35 U.S.C. §102 and/ or 35 U.S.C. §103.

Claim 9 was canceled without prejudice or disclaimer in Applicants' previous Amendment.

35 U.S.C. §102 REJECTIONS

The Examiner has FINALLY rejected claims 1, 8, 10-13 and 19-21 under 35 U.S.C. §102(e) as being anticipated by Ino et al. [USP 6,424,328; "Ino"]. Applicants respectfully request reconsideration and allowance of Claims 1, 8, 10-13 and 19-21.

CLAIMS 1, 8 and 10-12

Claims 1, 8, and 10-12 stand rejected as being anticipated by the Ino reference. Applicants respectfully submit that the Examiner has read disclosure into the Ino reference that is not actually present therein by way of an inappropriate inherency argument. Accordingly, Applicants respectfully request reconsideration of the dispositive issue already present in this prosecution to which the Examiner's inappropriate inherency argument applies as will more fully appear below.

As was noted in the previous Amendment in this application, in Claim 1 Applicants claim a display device including an active matrix substrate, a counter electrode, a display medium layer interposed between the active matrix substrate and the counter electrode, and a plurality of pixels. The active matrix substrate includes, *inter alia*, a plurality of pixel switching elements each provided with a gate line to control the operations thereof; a plurality of data lines and a plurality of data line switching elements. Each data line is connected to associated ones of the pixel electrodes by way of associated ones of the pixel switching elements so as to supply a data signal therethrough; and a control line is connected to the data line switching elements.

In the presently claimed invention, signals are sent over the gate lines to selectively turn ON or OFF the pixel switching elements and signals are sent over the control line to selectively turn ON or OFF the data line switching elements. In particular, as described in numerous places within the subject application (*e.g.*, see page 11, paragraph [0017]), the signals to turn ON the data line switching elements and a signal to turn ON the pixel switching elements have mutually different polarities and the data lines and pixel electrodes are formed on the same substrate.

The present specification also indicates that a capacitance associated with the data line switching elements causes a potential level on the data lines to be raised (or dropped); and a capacitance associated with the pixel switching elements causes a potential level at the pixel electrodes to be dropped (or raised). In the present invention, a potential rise (or drop) caused by the operation of a data line switching element is substantially canceled by a potential drop (or rise) caused by the associated pixel switching element. As a result, the extent of any change in the voltage being applied to the display medium when the switching elements are turned from ON to OFF is reduced in comparison to the case in which a potential rise (or drop) is caused by the operation of both the data line switching element and the pixel switching element residing on the same substrate.

In the previous Official Action the Examiner asserted that in an active matrix substrate context similar to that of herein claimed (i.e., the Ino reference) it is disclosed that a signal to turn ON the data line switching elements and a signal to turn ON the pixel switching elements, respectively, have mutually different polarities as herein claimed. Applicants previously disagreed with the Examiner's characterization of what Figure 16 of the Ino reference, and particularly the elements designated therein by the reference items Q(n), SL1-SL3 and V_g in the Ino reference disclose. In the currently outstanding FINAL Official Action, however, the Examiner has indicated that the Applicants' arguments are not persuasive based upon an ***inherent*** disclosure in the Ino reference. Specifically, the Examiner now has indicated that:

> Applicant argues there is no discussion anywhere in Ino regarding Q(n) that discloses or describes that the signals are being applied to the data lines switching elements and the pixel switching elements to turn these elements ON have mutually different polarities. The Examiner disagrees because said mutually different polarities are ***inherent*** to the switching structure taught by Ino. The mutuality is governed by the switch control circuit 68 and the different polarities are governed by the image data output at Q(n) for each color that combines to form a pixel image. (Emphasis added)

The Examiner's change in emphasis from an explicit disclosure of the reference to an alleged inherent disclosure of the reference is significant. The M.P.E.P. makes this clear in section 2112 (IV) wherein it is stated;

> The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaret*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993)... *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA, 1981) "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient'" *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)...
> In relying upon a theory of inherency, the Examiner must prove a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. *Ex parte Levy*, 17 UISPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) – Emphasis in original

Applicants respectfully submit that the Examiner has failed to satisfy these standards in the present prosecution. Applicants also respectfully submit that to the extent that it might be said that the Examiner has established a *prima facie* case of inherent disclosure, that case has been overcome by Applicants detailed discussion of what the Ino reference actually discloses.

In particular, the item identified as Q(n) in the Ino reference **does not** represent a switching control voltage that is being applied to the data line switching elements and the pixel switching elements in Ino. Rather, as is explained in col. 11, lines 4-25 of the Ino reference, Q(n) is the output of the device driver IC 67 that is provided to the data lines. The polarity of Q(n) in the Ino reference is the same as that of VCOM within each scanning period 1H and also is

inverted every 1H. Further, ***Q(n) has the same polarity as the common voltage (VCOM) within each 1H***. Accordingly, the Examiner is correct to the extent that Q(n) in the Ino reference determines the polarity of the image data. However, there is absolutely no discussion anywhere in the Ino reference regarding Q(n) that discloses, describes or in any way definitively suggests that the signals being applied to the data line switching elements and the pixel switching elements to turn these switching elements ON are to have mutually different polarities.

The Examiner now apparently agrees, but nevertheless argues that the feature that the polarities of the signals that are required to switch the data line and pixel switches ON are mutually different from one another ***is inherent in the Ino switching structure***. **Applicants respectfully submit that the Examiner's conclusion in this regard is not, and cannot be, supported as required in the above-quoted portion of the M.P.E.P., and also is factually in error.**

In Figure 16 of the Ino reference, SL1-SL3 are the switch control pulses or signals from the switch control circuit 68 that are applied sequentially to the data line switching elements of the corresponding red, green and blue pixel electrodes for each gate line selected by the vertical driving circuit 65 (See, Ino at Column 10, lines 20-21, indicating that the analog switches 66R, 66G and 66B serve as ***time-division switches*** that operate sequentially).

Thus, it will be seen that the item identified as Vg in Figure 16 of the Ino reference represents the selection pulse sent from the vertical driving circuit 65 to control the writing of the display data to the pixels (See, Ino, Column 9, lines 57-63) However, nowhere in the Ino reference is it described, taught or suggested that Vg and SL1-SL3 are controlled so that VG and SL1-SL3 have mutually different polarities when the pulses are outputted to turn ON the respective data line switching elements and the associated pixel switching elements.

As to the Examiner's current suggestion that Figure 16 of the Ino reference somehow ***inherently*** illustrates and/or teaches the relationship between SL1-SL3 and V_g herein claimed, Applicants respectfully submit that while the claimed relationship is theoretically possible in the context established by the Ino reference, the presently claimed relationship is not disclosed, taught, suggested or otherwise ***necessary*** to the operation of the Ino reference circuitry. Indeed, Applicants respectfully note that Figure 16 of the Ino reference specifically shows that when the data acquired during the second of the three samplings thereof regarding Q(n) (see Column 11, lines 5-6, of the Ino reference) is being outputted sequentially to the red, green and blue pixels associated with gate line 61m, Vg is high and SL1 is high when red display data is being outputted to the red pixel, V_g and SL2 are high when green display data is being outputted to the green pixel, and SL3 and V_g are high when blue display data is being outputted to the blue pixel. (Note: VCOM during the scanning period illustrated in Figure 16 of the Ino reference according to its accompanying specification should be low rather than high since VCOM is stated to have the same polarity as Q(n) during each scanning period.)

Thus, and contrary to the claimed invention, the Ino reference clearly shows that the *polarities* of the switching element control signals and the pixel switching signals sent respectively to the switching elements of the data lines and the pixel switches ***are the same, not different***. (Note also that Fig. 6 of the Ino reference is consistent with this in that a positive signal to a data line selection switch allows the passage therethrough of both positive and negative image data. Consequently, the polarity of the image data is not ***necessarily*** determinative of the nature of the switches chosen or of the polarities associated with SL1-SL3 and Vg)

Applicants also respectfully submit that the result of the foregoing showing that the polarities of the ON/OFF signals supplied to the pixel switches and to the date line switches is that the Ino reference operates/functions in a manner different than that disclosed by the present invention. In the latter regard, specific attention is respectfully directed to Column 11, lines 36-62, of the Ino reference wherein the problem of voltage fluctuations caused by the operation of the switches in conjunction with their respectively associated switching capacitances is recognized. Instead of attempting to cancel out the resultant voltage fluctuations as in the present invention, the Ino reference indicates that by ensuring that the fluctuations associated with each color are always associated with pixels of that color in the time division scheme adopted the undesirable color unevenness can be avoided. In other words, the Ino reference realizes that there is a switching capacitance voltage factor respectively associated with both the pixel switch and the data line switch that introduces a voltage fluctuation in the output of the respective

pixels. However, rather than attempting to minimize the fluctuation as in the present invention, the Ino reference always maintains the variation associated with each color with pixels of that color so as to avoid noticable color fluctuation – a very different approach than that disclosed and taught by the present invention.

Accordingly, Applicants respectfully submit that there are clear, definite and significant distinctions between the Ino reference and Claims 1, 8 and 10-12 of the present application that have been overlooked by the Examiner in the course of his improper attempt by an inherency argument to incorporate disclosure into the Ino reference that simply is not there. Consequently, reconsideration and allowance of Claims 1, 8, 10-12 in response to this communication are respectfully requested.

CLAIMS 13, 19-21

Claims 13 and 19-21 also stand rejected as being anticipated by the Ino reference. Applicants respectfully submit that the Examiner has misunderstood their previous argument in the currently outstanding FINAL Official Action, and that when he correctly understands Applicants' position he will agree that Claims 13 and 19-21 are patentable.

Claims 13 and 19-21 deal with a display device that includes a pair of substrates that is disposed so as to face each other and be spaced apart from each other, a display medium layer interposed between the pair of substrates, and a plurality of pixels, **where a plurality of *counter signal electrodes*, each of which extends in a column direction and through which a data signal is supplied, are formed on a first one of the pair of substrates**. This display device also includes a plurality of signal electrode switching elements, each of which is connected to associated one of the counter signal electrodes and controls supply of the data signal to the counter signal electrode.

The second of the pair of substrate includes a plurality of pixel electrodes arranged in matrix, each said pixel electrode being associated with one of the plurality of pixels, a plurality of pixel switching elements, each of which is connected to associated one of the pixel electrodes, a plurality of gate lines, which extend in a row direction and are used for controlling operations of the pixel switching elements and ***a plurality of common lines, each of which is connected to associated ones of the pixel electrodes by way of associated ones of the pixel switching elements***. In such a display device a signal to turn ON the signal electrode switching elements and a signal to turn ON the pixel switching elements has the same polarity.

The Examiner asserts that the Ino reference discloses having a plurality of counter signal electrodes through which data is supplied provided on the one of the pair of substrates and providing *inter alia* the pixel electrodes, gate lines and common lines on the other of the pair of opposing substrates. In support of this position, the Examiner relies on the discussion found at Col. 3, lines 11-24 of the Ino reference. Applicants respectfully submit that the Examiner's

characterization of what is being disclosed at the reference point of the Ino reference is not correct.

Specifically, the portion of the Ino reference referred to by the Examiner provides that the display section is made up of gate lines, signal lines and pixels formed on a first transparent substrate, and on the other transparent substrate there is formed an opposite electrode. It is clear from the further discussion in col. 5, lines 23-27 and col. 9, lines 32-39 of the Ino reference that the opposite electrode is the electrode to which is applied the common voltage VCOM. As such, the assertion that the opposite electrode corresponds to the plurality of counter signal electrodes of the presently claimed display device is incorrect. Consequently, since the opposite electrode described by the Ino reference is the electrode to which the common voltage is applied, the Ino reference cannot be held to disclose a device having a plurality of common lines (to which the common voltage is applied) located on the same substrate as the pixels, pixel switching elements and gate lines.

The Examiner now states:

> Applicant argues that the Ino fails to teach an opposite electrode. The Examiner disagrees because said opposite electrode is inherent to the structure of Ino as known in the art and used for the purpose of creating an electric field across the display element altering the display contrast to form an image.

Applicants respectfully submit that the Examiner's current remarks indicate that the Examiner has misunderstood the comments made by Applicants concerning this issue in the previous Amendment filed in this prosecution. Applicants do not assert, and have not asserted, that the Ino reference does not disclose a counter electrode. What Applicants do assert, however, is that the Ino counter electrode has the so-called COMM voltage applied to it. Applicants also assert that the structure claimed in Claim 13 of this application requires the so-called COMM voltage to be applied to the pixel electrode on the substrate opposite to that carrying the counter electrode while the data signal is applied to the so-called counter electrode. The respective electrical connections to the pixel electrode on one of the pair of substrates and to the counter electrode on the other of the pair of substrates of the so-called COMM voltage on the one hand and of the data signal on the other hand in the device of Claim 13, therefore, are reversed relative to the device disclosed in the Ino reference.

Applicants, therefore, do not deny (and in fact agree) that a pixel electrode on one of the substrates of the pair of substrates and a counter electrode on the other substrate of the pair of substrates are required for the creation of an electric field across the display element. In the Ino reference, the image data is applied to the pixel electrode while the COMM voltage is applied to the counter electrode. In present claim 13, the COMM voltage is applied to the pixel electrode while the image data is applied to the counter electrode. In both cases an electric field is present across the display element. The more important points, however, are that (1) the Ino reference does not disclose, teach or suggest a device having the electrical connection set up required by Claim 13, and (2) the Ino reference consequently does not disclose, teach or suggest that the

control pulses to the pixel and data switches respectively when the electrical set up is as claimed in Claim 13 should be such that those control pulses should have the same polarity such that the change induced in the electric field across the display element at the pixel electrode is the same as the change induced at the counter electrode.

In the latter regard, Applicants again note that the Ino reference contemplates an additive effect +/- on the potential across the display element arising from the operation of the switches, while the present invention attempts to negate these effects. Hence, it will be seen that the Examiner has misconstrued Applicants' Remarks concerning the foregoing issues in suggesting that Applicants were asserting the Ino reference has not counter electrode. Therefore, Applicants respectfully submit that when appropriately construed their previous Remarks clearly distinguish Claim 13 from the Ino reference.

Applicants further respectfully submit that the foregoing remarks distinguishing the display device of claim 13 from Ino, also apply to distinguish the display device of claim 19 and 21 and the method for driving a display device of claim 20 from the cited Ino reference. Reconsideration and a decision so holding in response to this communication is respectfully requested.

35 U.S.C. §103 REJECTIONS

Claims 2-7, 9 and 14-18 stand rejected under 35 U.S.C. §103 as being unpatentable over Ino et al. [USP 6,424,328; "Ino"] in view of Ichikawa et al. [USP 6,559,821; "Ichikawa"].

CLAIMS 2-7, 14-18

Claims 2-7 and 14-18 stand rejected under 35 U.S.C. §103 as being unpatentable over Ino et al. [USP 6,424,328; "Ino"] in view of Ichikawa et al. [USP 6,559,821; "Ichikawa"].

Each of claims 2-7 depend directly or ultimately from Claim 1 and each of Claims 14-18 depend directly or ultimately from claim 13.

Further, as indicated in the respective discussions above in connection with the §102 rejections of these claims, Applicants respectfully submit that the Ino reference does not disclose the display device as set forth in either of claim 1 or claim 13. It also is respectfully submitted that the Ino reference does not teach or suggest a display device as set forth in either of claims 1 or 13. In addition, Applicants respectfully submit that the Ino reference does not teach, suggest or offer any motivation to modify the display device disclosed in Ino so as to yield the display device as set for in either of claims 1 or 13, nor does the Ino reference provide any indication that such a modification would be reasonably successful. Accordingly, at least because of their dependency from base claim that is considered to be allowable, each of claims 2-7 and 14-18 are considered to be allowable over the combination of Ino and Ichikawa.

Applicants, therefore, respectfully submit that for at least the foregoing reasons, claims 2-7 and 14-18 are patentable over the cited reference(s) and satisfy the requirements of 35 U.S.C. §103. Accordingly, it is believed that these claims are allowable. A decision so holding in response to this communication is respectfully requested.

In view of the foregoing Remarks it is respectfully submitted that the subject application is in a condition for allowance. Accordingly, since this submission is believed to place this application ion condition for allowance as required by 37 CFR 1.116 and since the foregoing Remarks do not introduce any new issues into this prosecution that would require further consideration and/or search by the Examiner, reconsideration and allowance of this application is response to this communication is respectfully requested.

Applicants believe that additional fees are not required for consideration of the within Response. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, the Commissioner is hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully submitted,

Date: October 13, 2004 By: _____

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